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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/964,010	09/26/2001	Matthew B. Haycock	884.455US1	1876

21186 7590 04/13/2006

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EXAMINER	
CHEN, TSE W	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 04/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/964,010	HAYCOCK ET AL.	
	Examiner	Art Unit	
	Tse Chen	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10-22,31,32 and 34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-22,31,32 and 34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 September 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on February 2, 2006 has been entered.

2. Claims 10-22, 31-32 and 34 are presented for examination.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "plurality of output bits at the corresponding output node is a copy of the plurality of input bits at the corresponding input node" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the

renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

4. A series of singular dependent claims is permissible in which a dependent claim refers to a preceding claim which, in turn, refers to another preceding claim. Claim 15 depends on claim 10, but is separated by independent claim 14.

A claim which depends from a dependent claim should not be separated by any claim which does not also depend from said dependent claim. It should be kept in mind that a dependent claim may refer to any preceding independent claim. In general, applicant's sequence will not be changed. See MPEP § 608.01(n).

5. Claim 18 is objected to because of the following informalities: "including," should be "including:". Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 10-17, 31-32 and 34 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are: means for establishing the reference plurality of bits to be aligned. Applicant claims that the plurality of output bits provided by one

output node are to be aligned with a plurality of output bits provided by other output nodes. Absent of any expected pattern to be used as a reference, it is not clear how the plurality of output bits provided by one output node can be aligned with a plurality of output bits provided by other output nodes [i.e., alignment must be based on some referential framework, particularly in the case of separate input nodes as defined by Applicant]. In the interest of compact prosecution, Examiner will assume the plurality of output bits of all the output nodes to be of the same pattern [i.e., universal reference] in order to apply prior art.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 10, 15 and 31 are rejected under 35 U.S.C. 102(b) as being anticipated by Wood et al., US Patent 4246656, hereinafter Wood.

10. Wood discloses an integrated circuit [diversity switch correlation circuit] comprising [fig.1; col.4, l.59 – col.5, l.53]:

- A plurality of input nodes [42, 44].
- A plurality of output nodes [72, 74].
- A plurality of register circuits [50/54 and 52/56], each of the register circuits being connected between a corresponding input node of the plurality of input nodes and a corresponding output node of the plurality of output nodes [e.g., 50/54 between 42 and 72] to receive a plurality of input bits at the corresponding input node and to provide at

the corresponding output node a plurality of output bits based on the plurality of input bits [col.5, ll.65-66; output bits on 72, 74 derived from input bits on 42, 44], each of the register circuits including a plurality of conductive paths connected between the corresponding input node and the corresponding output node [lines 62], wherein the plurality of output bits at the corresponding output node is a copy of the plurality of input bits at the corresponding input node [output bits 72, 74 is correctly aligned stream of input bits 42, 44].

- A logic circuit [66, 58, 60 with associated circuitries] connected to the register circuits to perform a logic function [compare] on the plurality of input bits held by one of the register circuits with the plurality of input bits held by the other register circuits among the plurality of register circuits [bits in both registers compared to find correlation].
- A controller to configure the register circuits based on a result from the logic circuit to select only one conductive path among the plurality of conductive paths of each of the register circuits to align the plurality of output bits provided by one output node with a plurality of output bits provided by other output nodes when the plurality of input bits received at the input nodes are misaligned with the plurality of input bits received at the other input nodes by one or more bit time intervals [58 configures 54 to select appropriate lines 62, 64 of respective registers for aligning the data streams].

11. As to claim 15, Wood discloses, wherein the logic circuit is configured to perform an OR function [196].

12. In re claim 31, Wood discloses a method comprising [fig.1; col.4, l.59 – col.5, l.53]:

- Receiving a plurality of input bits at a plurality of input nodes [42, 44] of a plurality of register circuits [shift register 50/mux 54 and shift register 52/mux 56 constitutes register circuits].
- Providing a plurality of output bits at a plurality of output nodes [72, 74] of the register circuits, wherein each of the register circuits includes a number of register cells [8 bits] connected to a corresponding input node of the plurality of input nodes [e.g., 50/54 between 42 and 72], a select circuit [54, 56] having input nodes connected to only a subset of the number of register cells through a number of select lines [62, 64], the select circuit having an output node connected to a corresponding output node [72, 74] of the plurality of output nodes of the register circuits, wherein the subset of the number of register cells [selected one cell associated with line 62] is less than the number of register cells, wherein the number of select lines [one line 62] is less than the number of the register cells [col.5, ll.54-55; only one line 62 is connected through selection to carry the on-line data].
- Performing a logic function [compare] on a plurality of bits held by the register circuits to produce a rotation number [three bit errors require advancing or retreating in rotation number of three bits in order to find correlation], wherein a plurality of bits held by the register circuits are based on the plurality of input bits [col.5, ll.65-66; output bits on 72, 74 derived from input bits on 42, 44].
- Aligning a plurality of output bits, based on the rotation number, when the plurality of input bits received at the input nodes are misaligned by at least one bit time interval

[correlating and selecting appropriate mux line based on the advancing or retreating rotation aligns the output bits].

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 11-13, 32 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wood as applied to claims 10 and 31 above, and further in view of Fukuoka, US Patent 6467063.

15. In re claims 11 and 32, Wood discloses each an every limitation of the claim as discussed above in reference to claims 10 and 31. Wood did not discuss the details regarding the number of register cells as related to the maximum number of bit timer intervals of misalignment.

16. Fukuoka discloses a circuit [Reed Solomon coding apparatus] comprising:

- Register circuits [90-97] that include a number of register cells, wherein the number of register cells equals 2M-1 [2s-1], where M [s] is a maximum number of bit time intervals of misalignment [maximum number of errors] [col.14, ll.48-60].

17. It would have been obvious to one of ordinary skill in the art, having the teachings of Fukuoka and Wood before him at the time the invention was made, to modify the system taught by Wood to include the register circuits taught by Fukuoka, in order to obtain the claimed integrated circuit wherein each of the register circuits includes a number of register cells, wherein the number of register cells equals 2M-1, where M is a maximum number of bits time intervals of misalignment of a parallel bus that connects to the integrated circuit. One of ordinary

skill in the art would have been motivated to make such a combination as it provides a way to correct multiple errors in a processing system [Fukuoka: col.1, ll.6-15].

18. As to claim 12, Wood discloses, wherein each of the register circuits further includes a select circuit [54, 56] connected to only a subset of the number of register cells through a number of select lines [62, 64], wherein the subset of the number of register cells [selected one cell associated with line 62] is less than the number of the register cells [8 bits], and wherein the number of select lines [one line 62] is less than the number of the register cells [col.5, ll.54-55; only one line 62 is connected through selection to carry the on-line data]..

19. As to claims 13 and 34, it would have been obvious to one of ordinary skill in the art, to further modify the system taught by Fukuoka and Wood in order to obtain the claimed integrated circuit wherein the number of select lines equals a maximum number bit time intervals of misalignment of a parallel bus that connects to the integrated circuit. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to select and process particular sets of data bits [Wood: col.3, ll.40-55; associate select lines with M since there's no need to further process bits greater than the maximum error].

20. Claims 14 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wood, in view of Yamamoto and Fukuoka.

21. In re claim 14, Wood discloses an integrated circuit [diversity switch correlation circuit] comprising [fig.1; col.4, l.59 – col.5, l.53]:

- A plurality of input nodes to receive a plurality of input bits [42, 44].
- A plurality of output nodes to provide a plurality of output bits [72, 74].

- A plurality of register circuits [50/54 and 52/56], each of the register circuits being connected between one of the input nodes and one of the output nodes [e.g., 50/54 between 42 and 72], each of the register circuits including a number of register cells [8 bits], each of the register circuits further including a select circuit [54, 56] connected to a subset of the number of register cells through a number of select lines [62, 64], wherein the subset of the number of register cells [selected one cell associated with line 62] is less than the number of the register cells [8 cells], and wherein the number of select lines [one line 62] is less than the number of register cells [col.5, ll.54-55; only one line 62 is connected through selection to carry the on-line data].
- A logic circuit [66, 58, 60 with associated circuitries] connected to the register circuits to perform a logic function [compare] on a plurality of bits held by the register circuits, wherein the logic circuit includes:
    - A calculation unit to perform the logic function on a plurality of bits [66 compares the bits from the different data streams to detect correlation].
    - A plurality of memory units to store results from the logic function [58, 60 stores the uncorrelated results from 66].
    - A counter to count values stored in the memory units [58, 60 counts uncorrelated results from 66].
    - A detect logic to determine results from the counter and to generate a rotation number [58, 56 determines the rotation number to advance or retreat by bits in order to align].

- A controller to configure the register circuits based on a result from the logic circuit to align the plurality of output bits provided by one output node with a plurality of output bits provided by other output nodes when the plurality of input bits received at the input nodes are misaligned by one or more bit time intervals [58 configures 54 to select appropriate line for aligning the data streams].

22. Wood did not discuss the details involved with rotating the data held in the number of register cells or the details regarding the number of register cells as related to the maximum number of bit timer intervals of misalignment.

23. Yamamoto discloses an integrated circuit [abstract, accompanying figure] comprising:

- A detect logic [5] to generate a rotation number [shift 1 bit], the rotation number being used to rotate data held in the number of register cells [paragraphs 0012-0013; when bits in 2 and 4 do not align, circuit configures by continually shifting and comparing bits until alignment].

24. It would have been obvious to one of ordinary skill in the art, having the teachings of Wood and Yamamoto before him at the time the invention was made, to modify the system taught by Wood to include the logic circuit and controller taught by Yamamoto, in order to obtain the claimed integrated circuit comprising a detect logic to determine results from the counter and to generate a rotation number, the rotation number being used to rotate data held in the number of register cells. One of ordinary skill in the art would have been motivated to make such a combination as it provides a very well known way to access particular bits of data [rotating] while synchronizing data streams with simplicity and reduction in current consumption [Yamamoto: abstract].

25. Fukuoka discloses a circuit [Reed Solomon coding apparatus] comprising:

- Register circuits [90-97] that include a number of register cells, wherein the number of register cells equals 2M-1 [2s-1], where M [s] is a maximum number of bit time intervals of misalignment [maximum number of errors] [col.14, ll.48-60].

26. It would have been obvious to one of ordinary skill in the art, having the teachings of Fukuoka and Wood before him at the time the invention was made, to modify the system taught by Wood to include the register circuits taught by Fukuoka, in order to obtain the claimed integrated circuit wherein each of the register circuits includes a number of register cells, wherein the number of register cells equals 2M-1, where M is a maximum number of bits time intervals of misalignment of a parallel bus that connects to the integrated circuit. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to correct multiple errors in a processing system [Fukuoka: col.1, ll.6-15].

27. Furthermore, it would have been obvious to one of ordinary skill in the art, to further modify the system taught by Fukuoka and Wood in order to obtain the claimed integrated circuit wherein the number of select lines equals a maximum number bit time intervals of misalignment of a parallel bus that connects to the integrated circuit. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to select and process particular sets of data bits [Wood: col.3, ll.40-55; associate select lines with M since there's no need to further process bits greater than the maximum error].

28. As to claim 17, Wood discloses, wherein the counter [58, 60] includes a plurality of counter memory units [2 units], each of the counter memory units being connected to one shift register [58/50 and 60/52].

29. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wood, Yamamoto and Fukuoka as applied to claim 14 above, and further in view of Taya et al., US Patent 5778214, hereinafter Taya.

30. Wood, Yamamoto and Fukuoka did not disclose explicitly to arrange memory units in rows and columns, wherein the memory units in the same row form a shift register.

31. Taya discloses an integrated circuit [2] wherein the memory units [22a-c] are arranged in rows and columns, wherein the memory units in the same row form a shift register

32. It would have been obvious to one of ordinary skill in the art, having the teachings of Taya, Wood, Yamamoto and Fukuoka before him at the time the invention was made, to modify the system taught by Wood, Yamamoto and Fukuoka to include the explicit teachings of Taya, as the configuration disclosed by Taya is extremely well known and suitable for use in the system of Wood, Yamamoto and Fukuoka. One of ordinary skill in the art would have been motivated to make such a combination as it provides an extremely well known way to store information [Taya: col.2, ll.51-62; memory configuration stores bits to be compared in Wood].

33. Claims 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moriwaki in view of Grondalski, US Patent 6108763 and Mani et al., US Patent 6034889, hereinafter Mani.

34. In re claim 18, Moriwaki discloses a system [rendering processing system] comprising:

- A parallel bus [internal data bus 15] including a plurality of bus lines to carry a plurality of bits on each of the bus lines [fig.5; col.9, ll.7-23].
- A first integrated circuit [data transfer circuit 12] including a plurality of register circuits [50-1 to 50-64], each of the register circuits being connected to one of the bus lines [col.9, ll.7-23].

- Each of the register circuits including:
- A register [set of three 24-bits 50-x registers combined for 64 bits] connected to an input node [inherently, an input node in the broadest interpretation is at the other end of the bus], the register including a plurality of register cells [set of 50-x registers] [col.9, ll.7-41].
- A select circuit [selector 51] connected to a subset of the number of register cells through a number of select lines [24b], the select circuit including an output node [switch circuit 52] [fig.5; col.9, ll.24-54].
- A controller [memory control circuit 4] connected to the select circuit and the register cells to configure the register cells to select the select lines to be a part of a conductive path connected between the input node and the select circuit output node [col.9, l.24 – col.10, l.17; selector selects the 64 bits to be connected].

35. Moriwaki did not disclose explicitly that the registers are to be shift registers, that only one of the select lines is to be selected, or that each of the register circuits are to have their individual select circuits.

36. Grondalski discloses a system [11] comprising:

- A plurality of register circuits [21], each of the register circuits including:
  - A shift register [52] including a plurality of register cells [fig.4; col.19, ll.40-54].
  - A controller [issues the sel cell signal] connected to the register cells to configure the register cells to select only one of the select lines [col.21, ll.12-56; sel cell signal corresponding to sel8 with associated transistors for particular register cell].

37. It would have been obvious to one of ordinary skill in the art, having the teachings of Moriwaki and Grondalski before him at the time the invention was made, to use the shift register taught by Grondalski for the system disclosed by Moriwaki as the shift register taught by Grondalski is a well known device suitable for use as the register of Moriwaki. One of ordinary skill in the art would have been motivated to make such a combination as it provides a well-known way to manipulate data in a processing system [Grondalski: col.19, l.40 – col.20, l.22].

38. Mani discloses a system [fig.8] comprising a select circuit [dl, dc] connected to only a subset of the number of register cells through a number of select lines [e.g., a4-a7], the select circuit including an output node [to mm], wherein the subset of the number of register cells is less than the number of register cells, and wherein the number of select lines is less than the number of the register cells [col.10, ll.18-45].

39. It would have been obvious to one of ordinary skill in the art, having the teachings of Mani and Grondalski before him at the time the invention was made, to use the select circuit taught by Mani for the system disclosed by Moriwaki, in order to obtain the system wherein the subset of the number of register cells is less than the number of register cells, and wherein the number of select lines is less than the number of the register cells. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to better access memory [Mani: col.4, ll.1-53; col.5, ll.51-67].

40. As to claim 19, Moriwaki discloses the system comprising a second integrated circuit [rendering operation circuit 2] connected to the parallel bus [fig.5].

41. As to claim 20, Moriwaki discloses the system wherein the parallel bus is formed on a circuit board, and the first and second integrated circuits are located in the circuit board [col.6, l.64 – col.7, l.22; on board wiring of bus].

42. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mani, Moriwaki and Grondalski as applied to claim 19 above, and further in view of Barnsley et al., US Patent 5430812, hereinafter Barnsley.

43. Mani, Moriwaki and Grondalski disclose each an every limitation of the claim as discussed above in reference to claim 19. Mani, Moriwaki and Grondalski did not discuss separate circuit board configuration.

44. Barnsley discloses a system [fig.5; digital image data compression apparatus] comprising:

- A first circuit board [pc 112], wherein the parallel bus [AT bus 118] is formed on the first circuit board and a first integrated circuit [80386] is located on the first circuit board [col.4, ll.53-68].
- A second circuit board [110], wherein a second integrated circuit [fractal transform chips] is located on the second circuit board, the second circuit board being inserted into a bus slot that connects to the parallel bus [col.4, ll.53-68].

45. It would have been obvious to one of ordinary skill in the art, having the teachings of Mani, Barnsley, Moriwaki and Grondalski before him at the time the invention was made, to use the circuit board configuration taught by Barnsley for the system disclosed by Mani, Moriwaki and Grondalski as the circuit board configuration taught by Barnsley is a well known configuration suitable for use with the system of Mani, Moriwaki and Grondalski. One of

ordinary skill in the art would have been motivated to make such a combination as it provides a well-known way to interconnect various parts in a processing system [Barnsley: col.4, ll.53-68].

46. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mani, Moriwaki and Grondalski as applied to claim 19 above, and further in view of Frisch et al., US Patent 4707834, hereinafter Frisch.

47. Mani, Moriwaki and Grondalski disclose each an every limitation of the claim as discussed above in reference to claim 19. Mani, Moriwaki and Grondalski did not discuss separate circuit board configuration.

48. Frisch discloses a system [instrument system] comprising a first and second integrated circuit [instruments 12] that are located on separate circuit boards, and the parallel bus [26] is not formed on the first or second circuit boards [col.4, ll.28-58].

49. It would have been obvious to one of ordinary skill in the art, having the teachings of Mani, Frisch, Moriwaki and Grondalski before him at the time the invention was made, to use the circuit board configuration taught by Frisch for the system disclosed by Mani, Moriwaki and Grondalski as the circuit board configuration taught by Frisch is a well known configuration suitable for use with the system of Mani, Moriwaki and Grondalski. One of ordinary skill in the art would have been motivated to make such a combination as it provides a well-known way to interconnect various parts in a processing system [Frisch: col.4, ll.28-58].

Response to Arguments

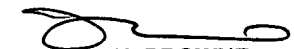
50. Applicant's arguments dated February 2, 2006 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Tse Chen
March 20, 2006